REMARKS

Upon entry of the amendment, claims 1-6, 8-13, and 14-16 are pending. Claim 7 has been cancelled. Claims 1-3, 5, 6, 8-12 and 14-16 have been amended to more particularly point out Applicant's invention.

SPECIFICATION:

Paragraph 1 of the Detailed Action identifies several typographical errors in the specification. These typographical errors are being corrected by way of the instant amendment. Accordingly, this objection should be obviated.

CLAIM OBJECTIONS:

Claims 1-3, 7 and 9-13 have been objected to as set forth in paragraph 1 of the Detailed Action. Each of these claims has been amended to overcome the objections set forth in paragraph 1 of the detailed action. Accordingly, these objections should be obviated.

CLAIM REJECTION - 35 U.S.C. §112:

Claims 9, 14, 15 and 16 have been rejected under 35 U.S.C. §112 as set forth in paragraph 2 of the Detailed Action. Each of these claims has been amended to overcome the rejection under 35 U.S.C. §112. Accordingly the Examiner is respectfully requested to reconsider and withdraw these rejections.

CLAIM REJECTIONS - 35 U.S.C. §102:

Claims 1, 2, 4 and 6-8 have been rejected under 35 U.S.C. §102(a) as being anticipated by Li, U.S. Patent No. 6,242,979. In order for there to be anticipation, each of the elements of the claims must be disclosed in a single reference, in this case the Li patent. In particular, claims 1, 2, 4, 6 and 8 relate to a predistortion amplifier that is adapted to be used with an upstream power amplifier whose characteristics are selected so that the output of the power amplifier is linear over the input power range. This is accomplished by selecting a predistortion circuit

configured as a Doherty power amplifier with characteristics that compensate for the characteristics of the upstream power amplifier. The Li patent discloses a topology in which a predistorted carrier amplifier is coupled in parallel with a main power amplifier. The predistorted carrier amplifier signal is predistorted. The signals are then combined by way of a signal combiner. The present invention relates to the serial connection of a Doherty amplifier and a power amplifier; a totally different configuration from that disclosed or suggested in the Li patent. For these reasons, the Examiner is respectfully requested to reconsider and withdraw this rejection.

CLAIM REJECTIONS – 35 U.S.C. §103(a):

Claims 3, 5 and 9-16 have been rejected under 35 U.S.C. §103(a) as being unpatentable over the Li patent in view of Gentzler U.S. Patent No. 6,211,733. The Gentzler patent simply relates to a predistortion compensation technique. Claim 6, as amended, recites a linear power amplifier that includes a power amplifier and an upstream predistortion circuit configured as a Doherty amplifier. These claims also recite that the predistortion Doherty amplifier and the power amplifier are serially connected. As discussed above, the Li patent teaches away from such a configuration and teaches a topology in which the predistortion amplifier is connected in parallel with the power amp. The Gentzler patent likewise does not disclose a topology as recited in the claims at issue in which the predistortion amplifier is serially connected to the power amplifier. Moreover, neither Li nor Gentzler discloses the use of a Doherty amplifier whose characteristics are selected to precompensate for non-linear characteristics of a power amplifier as recited in the claims at issue. For these reasons, the Examiner is respectfully requested to reconsider and withdraw the rejection of claims 3, 5, and 9-16.

Serial No. 09/878,104 TRW Docket No. 12-1101

CONCLUSION

In view of the foregoing remarks, Applicant respectfully requests reconsideration of this application and that the application be passed to issue.

Respectfully submitted,

Date: November 25, 2002

Noel F. Heal
Registration No. 26,074

TRW INC.
Intellectual Asset Management
One Space Park, E2/6051
Redondo Beach, CA 90278
Telephone: (310) 812-4910
FAX: (310) 812-2687

Serial No. 09/878,104 TRW Docket No. 12-1101

ATTACHMENT FOR SPECIFICATION AMENDMENTS
VERSION WITH MARKINGS TO SHOW CHANGES MADE
U.S. Serial No. 09/878,104; Filed June 8, 2001

Paragraph **[0017]** on page 4, was amended as follows:

[0017] In order for the output signals from the carrier amplifier 22 and the peak amplifier 24 to be in phase at the output, a Lange coupler 32 is provided. One input terminal of the Lange coupler 32 is used as a RF input port 34. The other input terminal is terminated to an input resistor 36. One output terminal of the Lange coupler 32 is coupled to the input of the carrier amplifier 22 while the other output terminal is coupled to the input to the peak amplifier 24. A [8/4] $\lambda/4$ impedance transformer having a characteristic impedance $Z_o = 2R_L + R_{opt}$ is provided at the output of the amplifiers 22 and 24. An output terminal of the power amplifier 20 is terminated to load impedance R_L. Both the carrier amplifier 22 and the peak amplifier 24 are configured to deliver maximum power when the load impedance R_L is R_{opt}.

Paragraph **[0020]** on page 5, was amended as follows:

[0020] The matching networks 26 and 28 are serially coupled to the outputs of the carrier and peak amplifiers 22 and 24, respectively. These matching networks 26 and 28 may be provided as low pass networks, for example, as illustrated in Figs. [3a-3c] 5A-5C. As shown in Figs. [3a-3c] 5A-5C, the matching networks 26, 28 may be implemented as a series inductance 40 or transmission line 42 and a shunt capacitance 44 or open stub 46. In operation, when the carrier amplifier 22 is on and the peak amplifier 24 is off, the matching networks 26, 28 provide a relatively high impedance (mainly due to the high impedance transmission line 42 or inductance 40) such that the peak amplifier 24 does not load down the carrier amplifier 22, operating in class A, to achieve optimum linearity and efficiency under low input power conditions.

Paragraph **[0022]** on page 5, was amended as follows:

[0022] Various biasing networks can be used for tuning the carrier and peak amplifiers 22 and 24. Exemplary biasing networks 48 and 50, are illustrated in Figs. [5A] 6A and [5B] 6B. Each of the biasing networks 48, 50 include a biasing resistor, R_{bbc} or R_{bbp}, coupled to an external source of DC, V_{bc} or V_{bp}. A low pass capacitor C_{clp} or C_{plp} is coupled to the biasing resistor, R_{bbc} or R_{bbp}, the external source DC voltage, V_{bc} or V_{vp}, and ground to filter out noise. Coupling capacitors C_{cc}, C_{cp} may be used to couple the carrier and peak amplifiers 22 and 24 to the Lange coupler 32.

Paragraph **[0023]** on page 5, was amended as follows:

[0023] The biasing circuits, for example, the biasing circuits 48 and 50, enable one or the other or both the carrier amplifier 22 and peak amplifier to be electronically turned. In the case of the exemplary biasing circuits 48 and 50, illustrated in FIGs. [5A] 6A and [5B] 6B, respectively, the biasing of the carrier and peak amplifiers 22 and 24 may be varied by varying the amplitude of the external DC voltage V_{bc}, V_{bp} coupled to the input of the carrier and peak amplifiers 22 and 24.

Serial No. 09/878,104 TRW Docket No. 12-1101

ATTACHMENT FOR CLAIM AMENDMENTS
VERSION WITH MARKINGS TO SHOW CHANGES MADE
U.S. Serial No. 09/878,104; Filed: June 8, 2001

1. (Amended) A predistortion circuit for a power amplifier, the predistortion circuit comprising:

a Doherty power amplifier having a carrier amplifier and a peak amplifier, each amplifier having a respective bias level, the bias levels for said Doherty power amplifier selected to provide for predistortion of predetermined characteristics of an RF signal, [said] the bias levels further selected to precompensate for distortion of said RF signal by an upstream serially connected power amplifier.

2. (Amended) The predistortion circuit as recited in claim 1, wherein one of said predetermined characteristics of the RF signal is gain as a function of input power level.

3. (Amended) The predistortion circuit as recited in claim 2, wherein the bias [level is] levels are selected to provide gain expansion as a function of input power.

5. (Amended) The predistortion circuit as recited in claim 4, wherein the bias [level is] levels are selected to provide phase compression as a function of input power level.

6. (Amended) A linear power amplifier circuit comprising:

a power amplifier having predetermined characteristics including input power range as a function of RF input power; and

an upstream predistortion circuit configured as a Doherty amplifier serially coupled to said power amplifier having characteristics selected to precompensate for said predetermined characteristics of said power amplifier as a function of input power.

8. (Amended) The linear power amplifier circuit as recited in claim [7] 6, wherein said power amplifier is configured as a Doherty amplifier having a predetermined gain compression characteristic as a function of input power.

9. (Amended) The linear power amplifier circuit as recited in claim 6, wherein said upstream predistortion circuit is configured to have a gain expansion characteristic such that the output gain of the circuit is relatively linear over the input power range of the power amplifier.

10. (Amended) The linear power amplifier circuit as recited in claim 6, wherein the power amplifier is configured as a Doherty amplifier having a predetermined phase compression characteristic as a function of input power.

11. (Amended) The linear power amplifier circuit as recited in claim 10, wherein said upstream predistortion circuit is configured to have a phase expansion characteristic such that the output gain of the circuit is relatively linear over the input range of the power amplifier.

12. (Amended) A linear power amplifier circuit comprising:

a power amplifier having predetermined characteristics including an input power range as a function of RF input power;

an upstream predistortion circuit for precompensating said predetermined characteristics of said power amplifier; and

means for electronically tuning said upstream predistortion circuit so that a predetermined characteristic of the linear power amplifier circuit is linear over the input power range of the power amplifier.

14. (Amended) The linear power amplifier circuit as recited in claim [6] 12, wherein said [tuning means includes means for electronically tuning the predistortion circuit

such that] predetermined characteristic is the output gain of the linear power amplifier circuit wherein said tuning means enables said output gain to be adjusted so that the output gain is relatively linear over the input range of the power amplifier.

15. (Amended) The linear power amplifier circuit as recited in claim [6] 12, wherein power amplifier is configured as a Doherty amplifier having a predetermined phase compression characteristic as a function of input power.

16. (Amended) The linear power amplifier circuit as recited in claim [12] 15, wherein said tuning means includes means for electronically tuning the predistortion circuit such that the output phase characteristic of the linear power amplifier circuit is relatively linear over the input range of the power amplifier.